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SPECIFICATION

TITLE OF THE DEVICE: Signal transmission circuit

SCOPE OF CLAIM:

A signal transmission circuit configured in a manner so that an input signal is supplied to a source-follower via a transmission gate, a first capacitance component for bootstrap is provided between the gate and source of said source-follower, and a signal from said source-follower is supplied to a transmission gate in the next stage, wherein said source-follower is constituted by a parallel circuit formed by a plurality of elements, and gate elements are provided respectively between said transmission gate and said plurality of elements constituting said source-follower, said gate elements being capable of being independently driven, thereby enabling detection and correction of defects.

DETAILED DESCRIPTION OF THE DEVICE

[Field for Industrial Use]

The present device relates to a signal transmission circuit suitable for the use as a scanning circuit for driving a CCD image pickup device, liquid crystal display and memory device etc.

[Summary Of The Device]

The present device relates to a signal transmission circuit comprising transmission gates and source-followers being connected in an alternating fashion, wherein the source-followers are constituted respectively by a plurality of elements so as to allow these elements to be driven independently to achieve detection of defects within the circuit as well as correction of such defects.

[Prior Art]

As for a signal transmission circuit used for a scanning circuit, the creator of the present device had previously proposed a circuit such as the one described below (Japanese Patent Laid-Open No. JP-A-177595/1983).

With reference to Fig. 3, an input terminal 1 is connected to the gate of an enhancement type MOS transistor M_{21} which is arranged in a source-follower construction via an enhancement type MOS transistor M_{11} constituting a transmission gate.

Herein, the MOS transistors are arranged as follows. With reference to Fig. 4, N^+-type source and drain regions (12) and (13) are formed over a P-type substrate (11). Over the surface of the element in an area between the source and drain regions (12), (13), an SiO_2 layer (14) is provided, and a gate electrode (15) is deposited thereon.

Accordingly, in a MOS transistor such as the one like this, a capacitor is formed in the region (16) located between

the gate electrode (15) and the source region (12) so as to provide a capacitance. Furthermore, when the gate potential increases, a channel (17) is formed between the source and drain regions (12), (13), and at this point, a capacitor is formed also between the gate electrode (15) and the channel (17).

This capacitor forms a capacitance component for bootstrap between the gate and source of the transistor M_{21} in the aforementioned circuit.

Furthermore, the drain of the transistor M_{21} is connected to the gate of an enhancement type MOS transistor M_{31} which constitutes a transmission gate. The source of the transistor M_{21} is connected to the gate of an enhancement type MOS transistor M_{41} via the drain-source of the transistor M_{31}. A capacitance component for bootstrap is provided between the gate and source of this transistor M_{41}. The drain of the transistor M_{41}, in turn, is connected to the gate of an enhancement type MOS transistor M_{12} constituting a transmission gate as a part forming the next stage circuit, and the source of the transistor M_{41} is connected to the drain of the transistor M_{12}.

This arrangement of the transistors M_{11}-M_{41} is connected repeatedly in a sequence.

Furthermore, a clock terminal (4) is connected to the gate of the transistor M_{11} and the drains of the transistors M_{41}, M_{42}, ..., and a clock terminal (5) is connected to the drains

of the transistors M_{21}, M_{22},...

In this circuit, signals ϕ_1, ϕ_2, which are indicated by "A", "B" and "C" in Fig. 5, are supplied to the clock terminals (4) and (5), and the input terminal 1, respectively. Herein, the high level of the signals ϕ_1, ϕ_2, ϕ_{IN} is expressed by V_H, and the low level thereof is expressed by V_L. The pulses of the signals ϕ_1, ϕ_2, ϕ_{IN} are represented by reference numerals [11], [12], ..., [21], [22] as shown in the diagram. The threshold values of the MOS transistors are all represented by V_{th}.

Under this condition, the signal ϕ_{IN} is first transmitted through the transistor M_1 upon the pulse [12] of the signal ϕ_1, and the voltage V_1 ("D" in the diagram) of the gate 1 of the transistor M_{21} then becomes;

$$V_1=V_H-V_{th} \quad \ldots\ldots \quad (1)$$

Next, since the voltage V_2 ("E" in the diagram) of the source 2 of the transistor M_{21} initially satisfies;

$$V_1-V_2=V_H-V_L>V_{th} \quad \ldots\ldots \quad (2),$$

so that the transistor M_{21} turns on and the voltage V_2 then becomes;

$$V_2=V_L \quad \ldots\ldots \quad (3).$$

Upon the pulse [22] of the signal ϕ_2, the voltage V_1 is brought up by the bootstrap effect of the capacitance component of the transistor M_{21}, and it becomes;

$$V_1=V_H+C_B/(C_B+C_S)\cdot V_H \quad \ldots\ldots \quad (4);$$

where, "C_B" is the bootstrap capacitance and "C_S" is the stray capacitance of the gate of the transistor M_{21}, and at this point, when;

$$V_1-V_{th}\geq V_H \quad \ldots\ldots \quad (5),$$

then;

$$V_2=V_H \quad \ldots\ldots \quad (6),$$

and the pulse [22] is drawn out to the source 2 of the transistor M_{21}.

Furthermore, the transistor M_{31} is turned on in synchronization with the signal ϕ_2, and the voltage V_2 is also accumulated in the gate 3 of the transistor M_{41}. The voltage V_3 ("F" in the diagram) of this gate 3 being turned into;

$$V_3=V_H-V_{th} \quad \ldots\ldots \quad (7)$$

turns on the transistor M_{41}, and this causes the pulse 13 to be drawn out to the source 4 of the transistor M_{41} ("G" in the diagram).

In the same manner, pulses 23, 14, ... of the signals ϕ_1, ϕ_2 are also outputted to the outputs 7, 10, ... of the transistors M_{22}, M_{42}, ... ("I", "K", ... in the diagram).

Accordingly, in this circuit, the input signal ϕ_{IN} is sequentially transmitted, and those pulses are sequentially drawn out to the sources of the transistors M_{21}, M_{41}, M_{22}, M_{42}, ... These pulses may be used for sequentially driving, for example, horizontal scanning lines. "C_{L1}", "C_{L2}", ... represent loads to which the pulses are supplied.

In the above-explained waveform diagram, the voltage rise V_A of the voltages V_1, V_3, V_5, ... is what is caused by the bootstrap effect of the capacitance components of the transistors M_{21}, M_{41}, ..., and it is given by;

$$V_A = C_B/(C_B+C_S) \cdot (V_H-V_L) \quad \ldots\ldots \quad (8).$$

The residual voltage V_E of the voltages V_2, V_4, ... is given by;

$$V_E = C_S/(C_S+C_L) \cdot (V_H-V_L) \quad \ldots\ldots \quad (9).$$

Assuming the use of capacitive load of a CCD image pickup device or a liquid crystal display etc. as for the load, then;

$$C_L \gg C_S,\ C_B \quad \ldots\ldots \quad (10),$$

so that the residual voltage V_E would become approximately zero, and it would cause no inconvenience in the normal operation.

As for the capacitance C_B as the capacitance component for bootstrap, from the above equations (4) and (5);

$$V_{H'}+C_B/(C_B+C_S) \cdot V_H - V_{th} \geq V_H \quad \ldots\ldots \quad (11)$$

may be derived, and where the withstand voltage of the transistors M_{11}, M_{31}, M_{12}, ... that constitute transmission gates is expressed by B_V, then;

$$B_V \geq V_{H'}+C_B/(C_B+C_S) \cdot V_H \quad \ldots\ldots \quad (12)$$

is given. From these two equations, the capacitance C_B may be selected from the range;

$$(V_H-V_{H'}+V_{th})/(V_{H'}-V_{th}) \cdot C_S \leq C_B \leq (B_V-V_{H'})/(V_H+V_{H'}-B_V) \cdot C_S$$

$$\ldots\ldots \quad (13).$$

In this way the transmission of the input signal ϕ_{IN} is

performed. Using this circuit, since output signals are formed by the pulses extracted from the clock signals ϕ_1 and ϕ_2, overlapping of output signals may easily be eliminated by reducing the width of the pulses of the clock signals ϕ_1 and ϕ_2.

Moreover, since through current would never occur within the circuit, the power consumption is extremely small.

Furthermore, since it is a non-inverting circuit in which output signals may be obtained from the respective clock signals ϕ_1 and ϕ_2, the frequency of the clock signals may be reduced to one half of the frequency used in the inverting type circuit of the prior art, and this allows further reduction in power consumption.

In addition, since a single output may be formed by two elements, the configuration of the whole circuit may substantially be simplified, thus, the circuit may be fabricated more easily at lower cost.

According to the above circuit, since large load capacitances C_L are connected to the transistors M_{21}, M_{41}, ... that constitute the source-followers, large current would occur in these transistors. Accordingly, the channel width W of these elements has to be made large.

However, the increased channel width W of the elements could cause variation in the characteristics of the elements. Accordingly, one approach was discussed, in which the

transistors M_{21}, M_{41}, ... are respectively divided into a plurality of elements (M_{21a}, M_{21b}, M_{21c}, M_{41a}, M_{41b}, M_{41c},...) to achieve reduction in the variation between the elements.

However, even with this configuration, the variation would not be eliminated completely, so that what is attempted, for example, is to obtain an output waveform such as one indicated by the curve 2 of the characteristic diagram of Fig. 7 within the tolerance range of variation, and to design the circuit by using this waveform to achieve normal functioning of the circuit. Therefore, in a circuit formed by elements with smaller variation, output waveforms such as the curve 3 shown in the characteristic diagram can be obtained, and the circuit exhibits a characteristic that is better than what is required. The curve 1 indicates a waveform obtained in one with larger variation.

On the other hand, when a large number of elements are provided as mentioned above, there would be a larger risk of promoting defects such as gate leaks or short-circuiting between sources and drains due to pin holes that might be generated within the respective elements. Accordingly, even if a circuit is formed by elements with smaller variation, it is highly possible that the circuit does not function properly due to defects present in those elements, and this causes low production yield.

Now, in the case of such a circuit formed by elements

with smaller variation, for example, even if one of the three elements is blocked, the output waveform would only become one as shown by the curve 2, and would not cause any problem in its functionality. The present device is the one which took note of this fact.

[Problem The Device Attempt To Solve]

The prior art circuit was configured in the aforementioned way. Accordingly, the elements constituting the circuit were susceptible to variations and defects, thus, had a problem of low production yield and reliability.

[Means To Solve The Problem]

The present device is a signal transmission circuit, which is configured in a manner so that an input signal is supplied to source-followers (transistors M_{21}, M_{41}, ...) via transmission gates (transistors M_{11}, M_{31}, ...), and a first capacitance component for bootstrap is provided between the gate and source of each of the source-followers, and the signals from the source-followers are supplied to the respective transmission gates located within the next stages, wherein the each source-follower is constituted by a parallel circuit formed by a plurality of elements (transistors M_{21a}, M_{21b}, M_{21c}, M_{41a}, M_{41b}, M_{41c}, ...), and gate elements (transistors M_{X1}, M_{Y1}, ...) are provided respectively between the transmission gates and

the plurality of elements constituting the respective source followers, and the gate elements are configured so as to be driven independently to allow detection and correction of defects.

[Operation]

According to this circuit, a plurality of elements for constituting the respective source followers are provided, and at the same time, each of the elements are so configured that they can be driven independently, so that, for example, within a circuit formed by elements with smaller variation, any defect within any of the elements may be detected, and while blocking this element, such the defect may be corrected. Accordingly, the circuit, which would otherwise be rejected as being unusable due to the defect, may be made usable, so that production yield and reliability may be improved.

[Embodiment]

With reference to Fig. 1, transistors M_{21}, M_{41}, ..., are divided, respectively, into a plurality of transistors M_{21a}, M_{21b}, M_{21c}, M_{41a}, M_{41b}, M_{41c} (in the diagram, transistors M_{41a}-M_{41c} are not shown), and at the same time, transistors forming gates M_{X1a}, M_{X1b}, M_{X1C}, M_{Y1a}, M_{Y1b}, M_{Y1C}, ... are provided, respectively, between the transistors M_{11}, M_{31}, ... and the gates of the transistors M_{21a}-M_{21c}, M_{41a}-M_{41c}, ... The gates of these

transistors M_{X1a}, M_{X1b}, M_{X1c}, M_{Y1a}, M_{Y1b}, M_{Y1c}, ... are respectively connected to power terminals (3a), (3b), (3c). Also, portions of the wirings between the transistors M_{X1a}-M_{X1c}, M_{Y1a}-M_{Y1c} and the gates of the transistors M_{21a}-M_{21c}, M_{41a}-M_{41c} are arranged so that these portions are located adjacent to the wirings to the sources or the drains of the transistors M_{21a}-M_{21c}, M_{41a}-M_{41c}, ... as shown in this diagram or Fig. 2.

In this circuit, while in a normal operation, the high electric potential (V_{DD}) at all the power terminal (3a)-(3c) would cause the transistors M_{X1a}-M_{X1c}, M_{Y1a}-M_{Y1c}, ... to be all turned into a conduction state, and the circuit would operate in the same way as the prior art circuit.

On the other hand, while in the same operation state as the above, if a circuit formed by elements with smaller variation does not operate, there is a possibility that a defect is present in some portion of the transistors.

In this case, by first supplying clock signals ϕ_1, ϕ_2 and an input signal ϕ_{IN} while detecting the current values of the clock signals ϕ_1 and ϕ_2, a stage in which the defect has occurred may be detected based on the number of pulses of the clock signals ϕ_1 and ϕ_2 occurred after the signal ϕ_{IN} was supplied when the current values changed. Next, by turning the power terminals (3a)-(3c) into low potential sequentially one by one to detect instances of normal operation, the defective one of the transistors M_{X1a}-M_{X1c}, M_{Y1a}-M_{Y1c}, ... may be identified.

When the defective transistor is identified in this way, a laser trimmer device is used to break the two lines (one of the sets of two lines indicated within the broken circles in the diagram) of the defective transistor. In this way, the defective transistor is blocked, thus the defect is corrected.

As explained above, any defective transistor may be detected and corrected, so that those circuits that would otherwise be rejected as being not usable may be made usable, thereby achieving improved production yield and reliability.

As previously mentioned, such blocking of a single transistor per one stage would not cause any problem in the functionality of the circuit.

Where there are a number of defects, the above-explained steps may be performed repeatedly to sequentially make the corrections of the defects.

In addition, the use of transistors M_{X1a}-M_{X1c}, M_{Y1a}-M_{Y1c}, ... will also yield an effect of alleviating the withstand voltage of the transmission gates previously proposed by the creator of the present device (Patent Application No. 155780/1983).

Furthermore, the above-explained apparatus may be implemented in those devices using crystalline silicon, amorphous silicon, polysilicon, and other organic or inorganic materials.

[Effect of The Device]

According to the present device, since a plurality of elements are provided for constituting respective source followers, and at the same time, since each of the elements may be driven independently, a defect in any element of i.e. a circuit formed by elements with smaller variation may be detected, and this element may be blocked to correct the defect, so that those circuits that would otherwise be deemed unusable can be made usable, so that the production yield and reliability may be improved.

BRIEF DESCRIPTION OF THE FIGURES

Fig. 1 is a diagram illustrating an exemplary schematic of the present device.

Fig. 2 is a diagram illustrating another example of the present device.

Figs. 3-7 are diagrams illustrating a circuit that had previously been proposed by the creator of the present device.

DESCRIPTION OF REFERENCE NUMERALS

(1): input terminal

(3a)-(3c): power terminals

(4), (5): clock terminals

M: MOS transistor

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